Please replace the paragraph beginning on page 31, line 4 with the following rewritten paragraph:

--Since it can take eight clock cycles in a worst case to load all the data necessary for one pixel, a conflict may cause a missed pixel processing clock cycle. This can only happen in very special cases; e.g. starting up a new polygon, when the LOD changes on a polygon or when in a non-LOD mode.--

A10

Please replace the paragraph beginning on page 31, line 11 with the following rewritten paragraph:

--Through an exhaustive series of simulations it has been shown that very few clock cycles are missed and the process seldom requires clock delays. Most of the time the data is already in the cache waiting to be used. This fact is due to the nature of the texture and pixel coherency.--

A11

IN THE CLAIMS:

Please cancel Claims 1 and 11 without prejudice.

Please amend Claims 2, 7, 8 and 14 as follows:

2. (Amended) The system of claim 14, wherein the system further includes a texture addressing scheme for organizing the array of texels in main memory to group spatially related texels in one memory page.

Sub C1

A8

7. (Amended) The system of claim 19, wherein N is equal to four and said texture main memory is organized into a plurality of texel blocks each having one of four block texel cache memory identifier in accordance with the following criteria: each texel block consisting of at least one group of four contiguous texels, the texels in each group consisting of one of each of the per texel cache memory identifiers, and wherein said texture cache memory being partitioned into a plurality of rows corresponding to said plurality of block texel cache memory identifiers, each cache memory bank having at least one row corresponding to each of the four block texel cache memory identifiers.

Sub C3

A9

A9 cont. Cont C3

8. (Amended) The system of claim 19, wherein said cache controller includes N stages.

Sub B1

14. (Amended) A computer graphics processor system having the capability of mapping texture onto a three dimensional object in a scene being displayed, the system comprising:

a texture address calculator for generating texel addresses for a list of primitives being processed;

a texture main memory containing an array of texels, each texel having an address and one of N identifiers;

a texture cache memory having addresses partitioned into N banks, each bank containing texels transferred from said main memory that have the corresponding identifier;

A10

a texture cache controller for determining and requesting the necessary transfer of texels from said texture main memory addresses to said texture cache memory addresses; and

a texture cache arbiter for scheduling and controlling the actual transfer of texels from said texture main memory into the texture cache memory and controlling the outputting of texels for each pixel to a interpolating filter from the cache memory, said cache arbiter coupled between said controller and said texture cache memory for determining which texels in the cache memory can be overwritten when new texels are determined to be transferred to said cache memory by said cache controller.

Please add a new Claim 19 as follows:

Sub B2

--19. (New) A computer graphics processor system having the capability of mapping texture onto a three dimensional object in a scene being displayed, the system comprising:

A11

a texture address calculator for generating texel addresses for a list of primitives being processed;

a texture main memory containing an array of texels, each texel having an address and one of N identifiers;